龙芯中科

3A6000

V1.5

[ ]

3A6000 ر 3A6000 ر ٥

أ

1.

1 32

2 32 64

SoC 3

64 IO

3A6000 4 8 FCBGA-1190

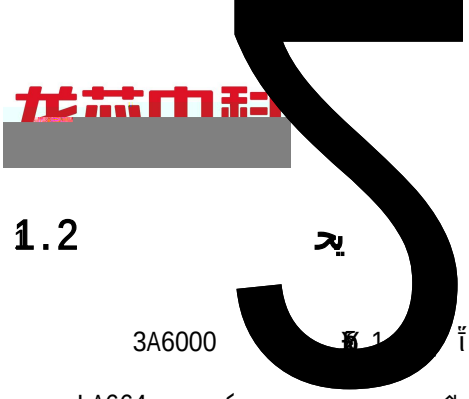
2.0GHz - 2.5GHz

1.1

1.1

	2.0GHz - 2.5GHz
	240GFlops@2.5GHz
	4
	8
	64 LA664 LoongArch ® 128/256 4 4 4
	64KB 64KB 256KB 16MB
	2 72 DDR4-3200 ECC
I/O	1 HyperTransport 3.0 IO HTO
I/O	1 SPI 1 UART 2 I2C 1 AVS 16 GPIO
	FCBGA1190
	38W@2.5GHz

1.2



3A6000 ... LA664 ...

1.2

1.5

3A6000

W

ث

1.2

1.6

1-2 غ

PMON	نهـ ضي كح
UEFI	نهـ ضي كح
GMAC	ا كح
GPIO	" î ¡ m "

1.7.2

LoongArch

1.7.3

1

PMON UEFI

2

Loongnix

1.8

1.8.1

O n n

1.8.2

16 ’hxxx 2 ’bxx 10 DDR_DQ0, DDR_DQ1, … DDR_DQ[31:0]

1.8.3

[O].[O]

chip_config0.uart_split

0 chip_config0 uart_split

2.

3A6000 1190

.....HyperTransport

.....DDR4 SDRAM

.....

.....I/O

.....

.....JTAG

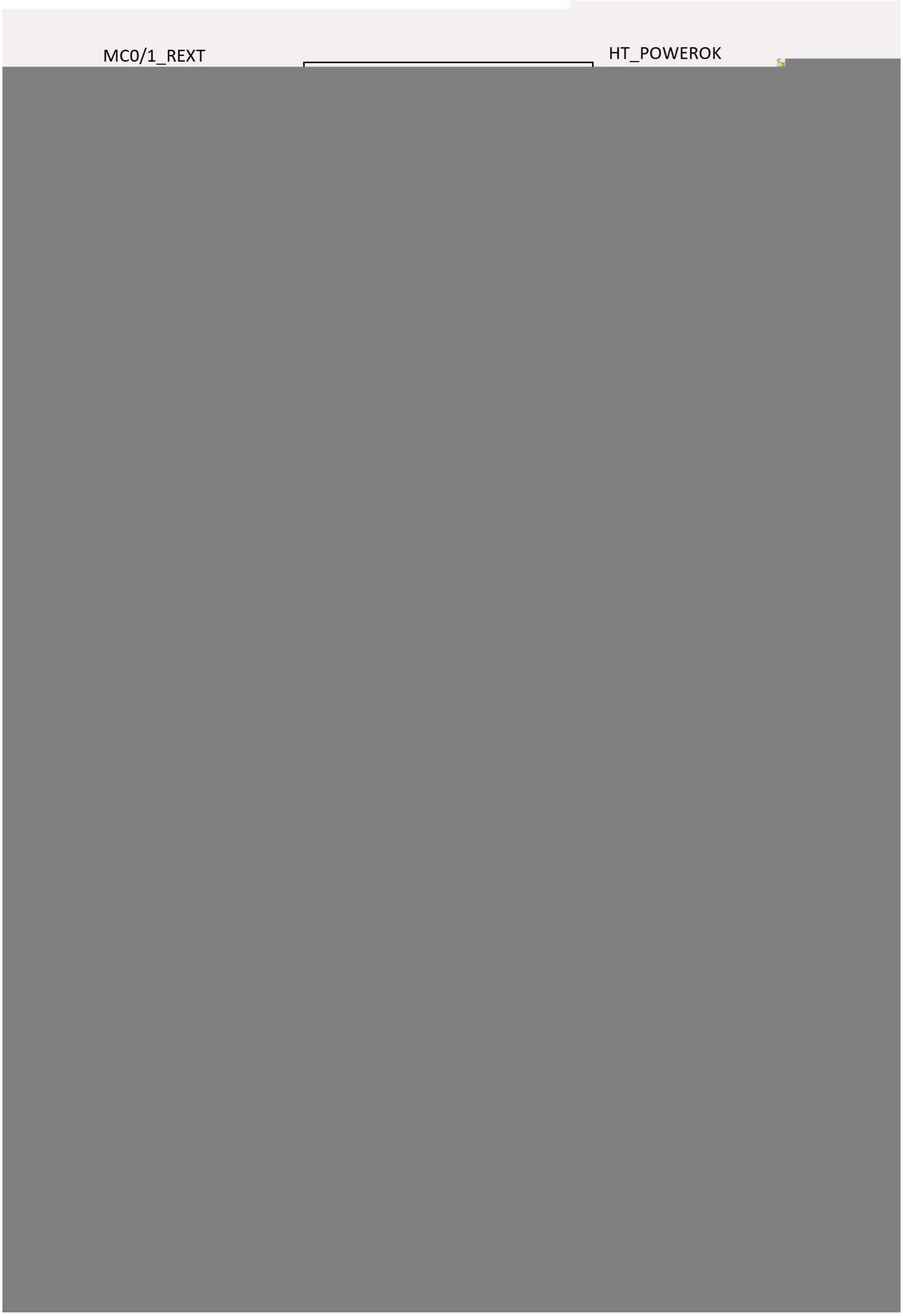
.....

.....

.....GPIO

.....SE

2.1



2.1

2.2

2.1

I
0
I/0
A

HT_Ldt_reqn	A6	I/O	HT Ldt_Reqn ˜	VDDE_IO	
HT_Tx_CADp[15:0]	C10 A11 C12 A13 C14 A15 C16 A17 G10 E11 G12 E13 G14 E15 G16 E17	O	HT Ũ ث	VDD_HT	
HT_Tx_CADn[15:0]	D10 B11 D12 B13 D14 B15 D16 B17 H10 F11 H12 F13 H14 F15 H16 F17	O	HT Ũ ث	VDD_HT	
HT_Tx_CTLp[1:0]	C8 G8	O	HT Ũ ˜	VDD_HT	
HT_Tx_CTLn[1:0]	D8 H8	O	HT Ũ ˜	VDD_HT	
HT_Tx_CLKp[1:0]	A9 E9	O	HT Ũ	VDD_HT	
HT_Tx_CLKn[1:0]	B9 F9	O	HT Ũ	VDD_HT	
HT_Rx_CADp[15:0]	D20 B21 D22 B23	I	HT ث	VDD_HT	

	D24 B25 D26 B27 G20 E21 G22 E23 G24 E25 G26 E27				
HT_Rx_CADn[15:0]	C20 A21 C22 A23 C24 A25 C26 A27 H20 F21 H22 F23 H24 F25 H26 F27	I	HT ث	VDD_HT	
HT_Rx_CTLp[1:0]	D18 G18	I	HT ˆ	VDD_HT	
HT_Rx_CTLn[1:0]	C18 H18	I	HT ˆ	VDD_HT	
HT_Rx_CLKp[1:0]	B19 E19	I	HT	VDD_HT	
HT_Rx_CLKn[1:0]	A19 F19	I	HT	VDD_HT	
HT_REXT		I	HT ă 800	VDD_HT	

2.3.2DDR o ˆ

3A6000 DDR4 SDRAM ˆ 3DS x8 x16

DDR4 o ˆ

72 ĭ h ˆ ECC

9 ĭ h ˆ ECC

9

15 خي ضر ˆ

2 BANK خي ضر ˆ

2 BANK GROUP خي ضر ˆ

4 ˆ

4 ˆ

4 ˆ

4 ث ˆ

4 ODT(On Die Termination) ˆ

1 ث ˆ

1 أ ˆ

1 ˆ

DDR o ˆ 2.3 3A6000 ك o ˆ

2.3 DDR4 o ˆ

ˆ O	ˆ	/			
MC0_DQ[63:0]	AB1 AC3 AE2 AE1 AB3 AB2 AD1 AE3 AG1 AH3 AK2 AK1 AG3 AG2 AJ1 AK3 AM1 AN3 AR1 AT2 AM3 AM2 AP1	I/O	ˆ	VDDIO_DDR	

~ O	~	/
	AR2	
	AU4	
	AR5	
	AT7	
	AU7	
	AR4	
	AT4	
	AU6	
	AR7	
	AR30	
	AR31	
	AU33	
	AT33	
	AT30	
	AU30	
	AR32	
	AR33	
	AR35	
	AT36	
	AN36	
	AN37	
	AU35	
	AT35	
	AP37	
	AN35	
	AL37	
	AK35	
	AH36	
	AH37	
	AL35	
	AL36	
	AJ37	
	AH35	
	AF37	
	AE35	
	AC36	
	AC37	
	AF35	
	AF36	
	AD37	
	AC35	

MCO 5

~ O	~	/
	AR11	
	AP11	
	AT9	
	AU9	
	AU11	
	AT	

[redacted]					
08 B ⊲> @	⅄ : : 8 ⅄	' Z	ƻ K 4!i .	ə. ' ZB . ɘ	
08 Bɘ(: ⅄	ⱸ3	ⱸ	ΓK: ŋ 9 e3+6ΓK ĘWΩ∓Q iWQ+6	ə. ' ZB . ɘ	
08 Bⱸ\ (ɘ⅄Ó	ⱸ8	' Z	⅄ ƻ 8ɘ8KI Ŀ - W¦ ÓbɪKI	ə. ' ZB . ɘ	
08 B3ⱸɘ	ⱸ⅄	Z	- > , b W¦ Óbɪ⅄	ə. ' ZB . ɘ	
08 Bⱸ8⅄Ó	ⱸ8	Z	⁰⁄₀ⱸK - .	ə. ' ZB . ɘ	
08 BɘHAHΛÓ	ⱸ3	Z	= } × ł .	ə. ' ZB . ɘ	
08 BZ, ⅄> @	ⱸɘ ⱸɘ ⱸ8 ⱸ⅄	Z	Z, ⅄ .	ə. ' ZB . ɘ	
08 B8 Ó> @	ⱸ⅄ ⱸɘ ⱸ3 ⱸɘ	Z	e 8⅂i EA* .	ə. ' ZB . ɘ	
08 B8 ɘ> @	ⱸɘ ⱸ3 ⱸɘ ⱸ⅄	Z	e 8⅂i EA* .	ə. ' ZB . ɘ	
08 B8 (> @	ⱸɘ ⱸ3 ⱸ8 ⱸɘ	Z	8⅂i _⅄- .	ə. ' ZB . ɘ	
08 Bɘ8ɘÓ> @	ⱸ⅄ ⱸ3 ⱸ3 ⱸ3	Z	(WĿə .	ə. ' ZB . ɘ	
08 Bɘⱸɘ Ó	ⱸ⅄	Z	>¦ , b Ŀə . Ę ⱸ	ə. ' ZB . ɘ	
08 B8ⱸɘ Ó	ⱸ8	Z	ɕ , b Ŀə . Ę ⱸ	ə. ' ZB . ɘ	
08 B (Ó	ⱸ8	Z	Ę _⅄- . Ę ⱸ	ə. ' ZB . ɘ	
08 B⁰⁄₀> @	ⱸ3 ⱸ⅄	Z	ĿKEA ⁰⁄₀ΩÓΛ0 , b .	ə. ' ZB . ɘ	
08 B⁰⁄₀> @	ⱸɘ ⱸ8	Z	ĿKEA ⁰⁄₀ΩÓΛ , b .	ə. ' ZB . ɘ	
08 Bⱸ	ⱸ8	Z	, b K 4!i .	ə. ' ZB . ɘ	
	ⱸ⅄ ⱸɘ ⱸɘ ⱸɘ				
	[redacted]				

~ O	~	/			
	T6				
	V7				
	W5				
	AA5				
	AB7				
	AD5				
	AD6				
	AA7				
	AA6				
	AC5				
	AD7				
	AF5				
	AG7				
	AJ5				
	AJ6				
	AF7				
	AF6				
	AH5				
	AJ7				
	AL5				
	AL6				
	AM8				
	AN8				
	AL8				
	AL7				
	AM7				
	AN7				
	AM27				
	AJ27				
	AK29				
	AJ29				
	AK27				
	AL27				
	AM29				
	AL29				
	AN33				
	AM31				
	AK33				
	AK32				
	AN31				
	AN32				
	AL33				
	AK31				

˜ O	˜	/			
	AH33 AG31 AE33 AE32 AH31 AH32 AF33 AE31 AC33 AC32 AA31 AA30 AC30 AC31 AA33 AA32				
MC1_CB[7:0]	AE10 AE9 AH10 AH11 AD10 AD9 AG11 AH9	I/O	ECC ˜	VDDIO_DDR	
MC1_DQSp[8:0]	V5 AC6 AH6 AN6 AJ28 AL32 AF32 AB30 AG9	I/O	´ ECC	VDDIO_DDR	
MC1_DQSn[8:0]	V6 AC7 AH7 AN5 AK28 AL31 AF31 AB31 AG10	I/O	´ ECC	VDDIO_DDR	
MC1_DM[8:0]	U5	O	DM0-8	VDDIO_DDR	

~ O	~	/
	AB5	
	AG5	
	AM5	
	AM28	
	AM33	
	AG33	
	AB33	
	AF9	

MC9

O		/			
	AJ17 AJ19 AM19				
MC1_ODT[3:0]	AL23 AL25 AM24 AK25	O	ODT	VDDIO_DDR	
MC1_Resetn	AL10	O		VDDIO_DDR	
MC1_ACTn	AL12	O		VDDIO_DDR	
MC1_PAR	AK20	O		VDDIO_DDR	
MC1_ALERTn	AK13	I/O	CRC	VDDIO_DDR	
MC1_REXT	AK10	A	240	VDDIO_DDR	

2.3.3 .

2.4 . O h

50KOhm

2.4 . o

<table>
<tr><th>O</th><th></th><th>/</th><th></th><th></th><th></th></tr>
<tr><td>SYSRESETn</td><td>M4</td><td>I</td><td>SYSCLK SYSCLK</td><td>VDDE_IO</td><td></td></tr>
<tr><td>CHIP_CONFIG[3:0]</td><td>L4
K4
J4
H3</td><td>I</td><td><table><tr><td>CHIP_CONFIG[0]</td><td>SE</td></tr><tr><td>CHIP_CONFIG[1]</td><td>HT Gen1</td></tr><tr><td>CHIP_CONFIG[2]</td><td></td></tr><tr><td>CHIP_CONFIG[3]</td><td>DCDL</td></tr></table></td><td>VDDE_IO</td><td>4'b0010</td></tr>
<tr><td>CHIP_CONFIG[9:4]</td><td>K3
K2
J2
J3
H1
H2</td><td>I</td><td><table><tr><th></th><th></th></tr><tr><td>[9]</td><td>1'b1 HT PLL CHIP_CONFIG[7]
1'b0 CHIP_CONFIG[7]</td></tr><tr><td>[8]</td><td>1'b1 HT PLL SYSCLK
1'b0 HT PLL</td></tr><tr><td>[7]</td><td>1'b0 PHY 6.4GHz
1'b1 PHY 0</td></tr></table></td><td></td><td></td></tr>
</table>

ضي SYSRESETn ╠ SYSRESETn Ա

كح ضي SYSRESETn كح كح

ضي 64K SYSCLK Ա U U

I2C UART AVS

I/O SPI Flash

17mA 35mA

2.5 SPI

2.3.5

3A6000 1 NMIn 16 GPIO

MSI HT

O h

GPIO INT0-3

NMIn

50KOhm

2.9

O		/			
NMIn	M8	I		VDDE_IO	

2.3.6JTAG o

3A6000 JTAG o

JTAG o w

JTAG O h 50KOhm

2.10 JTAG o

O		/			
TDI	V2	I	JTAG	VDDE_IO	
TDO	V3	O	JTAG	VDDE_IO	
TMS	W1	I	JTAG	VDDE_IO	
TRSTn	W3	I	JTAG	VDDE_IO	
TCK	W2	I	JTAG	VDDE_IO	
TSEL[1:0]	U2 U3	I	JTAG w 2'b00:LA664 JTAG 2'b01: JTAG	VDDE_IO	2'b00

2.3.7

3A6000 2.11 SYSCLK

HT_CLKp/HT_CLKn CHIP_CONFIG[9:4] 3A6000 Core

DDR SYSCLK CHIP_CONFIG[4] HT

HT HT_CLKp/HT_CLKn

SYSCLK CHIP_CONFIG[8] CHIP_CONFIG

SYSCLK

TESTCLK

CHIP_CONFIG

2.11

O / (MHz)	PLL
SYSCLK Y1 I 25/100	

GPIO ˜

ꝯ ˜ GPIO w ˜

ᾰ GPIO

˩ ʓ˜ ꝯ 17mA 35mA ᾰ

˩

2.13 GPIO ˜

GPIO	O	˜	w		ⅎ
0	GPIO00	M3	SPI_CSn1		VDDE_IO
1	GPIO01	K1	SPI_CSn2		VDDE_IO
2	GPIO02	L2	UART1_RXD		VDDE_IO
3	GPIO03	N3	UART1_TXD		VDDE_IO
4	GPIO04	L1	UART1_RTS		VDDE_IO
5	GPIO05	M2	UART1_CTS		VDDE_IO
6					

3. w ï o

3.1 HyperTransport o

3A6000 ç HyperTransport o IO HT o 16

3.1.1 o

HyperTransport o

HyperTransport 1.03/HyperTransport 3.0

IO o 200 - 3200MHz

IO Cache

3.1.2 o

3A6000 HT o IO

3.2 DDR o

3A6000 کل کل DDR4 SDRAM

JESD79-4

3.2.1 کل w

3A6000 کل کل 4 CS 2 CS

کل 2 کل 4

3A6000 ضي کل قمم ˜ کل ᾰ

ﻻ

CPU ΰ خي ضر کل   خي ضر

3A6000 کل 7 ἳ کل /

ضي /

3A6000 کل کل

o ث

ث

کل o ˜ ᾰ

DCC ˜ ΰ غ

ECC w ˜ 1 غ 2 1

خي ضر w

RDIMM UDIMM So-DIMM ἳ 3DS

x8 x16

133-800MHz

DDR4-3200

3.2.2 .

کل . U ˜ کل .

. h كح Init_start 0x010 1 ضي Init_start

ˆ ╠ كح

ㄱ DRAM .

(1) h كح Init_start 0x010 ضي

0

(2) Init_start 0x010 1 .

(3) PHY . DLL w ˆ

Dll_init_done 0x030 ˆ Dll_value_ck 0x030

╠ w . ˆ

Dll_bypass 0x030 .

(4) DLL bypass U كح DRAM . h DRAM

Ü . MRS ث ZQCL ث

(5) ˆ Dram_init 0x010 كح . ㄱ

3.2.3

ضي STR ¥ ㄱ ضر ˆ pad_reset_po 0x808

كح DDR_RESETn

(1) pad_reset_po[1:0] = 2 ' b00 ˆ

DDR_RESETn

كح .

2

STR 3

4.

4.1

3A6000 SPI Flash

4.2

DOTESTn CHIP_CONFIG

CHIP_CONFIG[4]

4.1

DOTESTn	w
CHIP_CONFIG[9]	HT
CHIP_CONFIG[8]	SYS_CLOCK HT
CHIP_CONFIG[7]	6.4GHz HT PLL VCO
CHIP_CONFIG[6]	
CHIP_CONFIG[5]	
CHIP_CONFIG[4]	

5.

5.1

3A6000 ǐ

SYS_CLOCK Ɏ SYSCLK

5.1 ฬ

Boot Clock	SYS_CLOCK	*1			SPI UART I2C ฬ
Main Clock	SYS PLL	PLL			SYS PLL Node Clock Core Clock HTcore Clock LA132 Clock Mem Clock Stable Clock˜
Node Clock	Main Clock	*1			HT ฬ
Core0 Clock	Main Clock	*1			0
Core1 Clock	Main Clock	*1			1
Core2 Clock	Main Clock	*1			2
Core3 Clock	Main Clock	*1			3
HTcore Clock	Node Clock	*1			HT ฬ U 1.25GHz
LA132 Clock	Main Clock	*1			LA132 U 1GHz
Stable Clock	SYS_CLOCK	*1			ฬ ฬ
Mem Clock 0/1	MEM PLL0	PLL			ฬ 0/1
	Main Clock	/2 /4 /8			ฬ 0/1

5.2

ฬ´ ǎ SYSCLK ǎ ₇

Ɏ˜ ˜

SYSCLK˜ 100MHz 25MHz

CHIP_CONFIG[4]

HT_CLKp/n˜ 200MHz

5.2 ǎ

˜ O	/	ח (MHz)		۱
SYSCLK	I	25/100	˫ PLL ڪ Core	VDDE_IO
HT_CLKp/ HT_CLKn	I	200	HT ǎ	VDD_HT

5.2.1 ۱

SYSCLK LVCOMS ڤمم 1.8v

		ڤمم			۱
V	۱				
Vih	۱	1.25			V
Vil	۱			0.4	V
Cin			2		pf
Tr	٦	1	2.2	3.6	V/ns
Tf					
Duty Cycle	\J		45% 55%		
Clock jitter	˫ multiple output frequencies switching		74		ps

Ø

5.3

ক PLL SYS PLL MEM PLL ę HT PLL

SYS PLL ę MEM PLL U SYS_CLOCK

S

6.

6.1

3A6000 ´ SYSRESETn ¿ HT o HT_powerok HT_resetn

SYSRESETn HT powerok HT resetn

ÇÉ ˆ SYSRESETn ╠ ˆ ¿ .

ˆ ˆ ´ ï ˆ ï ð

Ù ð SYSCLK

HT o HT_CLKp/n

. ˆ DOTESTn CHIP_CONFIG

SYSRESETn ï U ÇÉ .

*_PLL VDD_HT VDDIO_DRR VDDE_IO

3A6000 ± 25mV

7.

7.1 ǎ

7.1 ǎ

	(°C/W)
	0.726
	0.070
	0.656

z ǎ

LS3A6000-HV/LL/BLL 30KG

LS3A6000M 10KG

7.2 TDP

7.2 ǎ è

ǎ	
TDP Max Power LS3A6000-HV	80W
TDP Max Power LS3A6000-BLL	85W
TDP Max Power LS3A6000-LL	60W
TDP Max Power LS3A6000M	30W
T_c / T_j	70 °C / 85 °C

w w è

w Tj ǐ 1 w

7.3 ǐ

7.3

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C *	260 °C *	260 °C *
1.6 mm - 2.5 mm	260 °C *	250 °C *	245 °C *
> 2.5 mm	250 °C		

7.4 ※

Profile Feature		Pb-Free Assembly
Average ramp-up rate (Tsmax to Tp)		3 °C/second max.
Preheat	Temperature Min (Tsmin)	150 °C
	Temperature Max (Tsmax)	200 °C
	Time (Tsmin to Tsmax) (ts)	60-180 seconds
Time maintained above	Temperature (TL)	217 °C
	Time (tL)	60-150 seconds
Peak Temperature (Tp)		245 °C
Time within 5 °C of actual Peak Temperature (tp)2		20-40 seconds
Ramp-down Rate		6 °C/second max.
Time 25 °C to Peak Temperature		8 minutes max.

VDDP	مخ كح	0.9V

9.3 ẅ

9.3.1 ﻣﺨ ẅ

ﻙ ẅ ﺿﻲ VDDN ẅ ﺿﻲ

3 70 ﻻ ẅ

VDDIO_DDR ´ ﻬ ﺃ ẅ

3A6000 ü ´ ﻬ ﺃ UDIMM ﻹ 16GB HT ه 3.2GHz

9.5 ẅ

ddr Pvddp Pvdde_I

9.3.3 w

□ ㄧ □ VDDN w

ゑ 9.2 40 w

9.4

3A6000 Core IO

9.5 o

9.5.1HyperTransport o

HT o HT1.0 HT3.0 ゑ 200MHz — 3200MHz DC AC

HT1.0 200 - 800MHz ... HT1.03a ヽ

HT3.0 1000 — 3200MHz ... HT3.0 ヽ

9.5.2DDR o

DDR o DDR4 ... JESD79-4

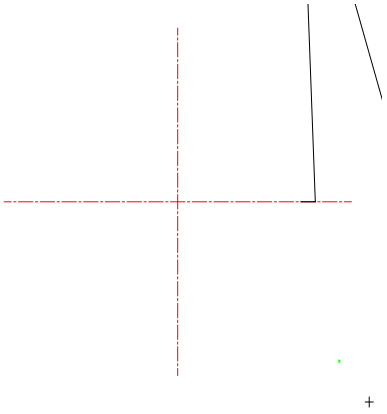
A2	1.142	1.272	1.402
A3	1.260	1.360	1.460
b	0.450	0.550	0.650
D/E	34.900	35.000	35.100
D1/E1		32.9184	
e		0.9144	
g/f		1.0408	
aaa		0.200	
ccc		0.350	
ddd		0.200	
eee		0.250	
fff		0.100	
N		1190	

NOTE:

1. DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2009.
3. TERMINAL POSMONS DESIGNATION PER JESD 95.

10.1.2 LS3A6000M

3A6000M ضي □ يح



NOTE:

1. DIMENSIONS ARE IN MILLIMETERS.

11. ج

11.1

3A6000 ث O

LS	3A	6000	-A
			ـِ -HV -BLL -LL M

11.2 3A6000 HV/LL/BLL

1 •

2 كِ LS3A6000

3 ج Cored By™ LA664

4 A ج

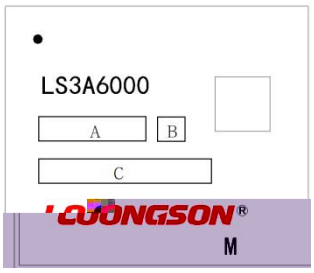
5 B

6 ٨ ـِ LOONGSON

7 C ج

8 ج

11.3 3A6000M



1 ●

2 LS3A6000

3 A B

4

5 C

6 LOONGSON

7 M M

引

	1	2	3	4	5
A			VSS A3	SE_QSPI_CLK A4	HT_POWEROK A5
B		VSS B2	SE_SPI_CLK B3	SE_I2C_SDA B4	SE_UART0_TX B5
C	VSS C1	SE_RNG0_CLK C2	SE_SPI_CSN C3	SE_I2C_SCL C4	SE_QSPI_IO3 C5
D	SE_RNG1_CLK D1	SE_RNG0_OEN D2	SE_SPI_MISO D3	SE_SPI_MOSI D4	SE_QSPI_IO0 D5
E	SE_GPIO02 E1	SE_GPIO00 E2	VDDE_IO E3	SE_RNG0_DATA E4	VSS E5
F	VSS F1	SE_GPIO01 F2	SE_GPIO05 F3	SE_RNG1_PE F4	SE_RNG1_OEN F5
G	SE_GPIO09 G1	SE_GPIO06 G2	SE_GPIO08 G3	SE_GPIO07 G4	SE_GPIO04 G5
H	CHIP_CONFIG8 H1	CHIP_CONFIG9 H2	CHIP_CONFIG3 H3	VDDE_IO H4	SE_CLK_SEL H5
J	VDDE_IO J1	CHIP_CONFIG6 J2	CHIP_CONFIG7 J3	CHIP_CONFIG2 J4	SPI_WPN J5
K	GPIO01 K1	CHIP_CONFIG5 K2	CHIP_CONFIG4 K3	CHIP_CONFIG1 K4	UART_TXD K5
L	GPIO04 L1	GPIO02 L2	VSS L3	CHIP_CONFIG0 L4	VSS_PLL_HT L5
M	VDDE_IO M1	GPIO05 M2	GPIO00 M3	SYSRESETN M4	VSS_PLL_SE M5
N	GPIO08 N1	GPIO06 N2			

Y	SYSCLK Y1	I2C1_SDA Y2	I2C1_SCL Y3	VSS Y4	VSS Y5
AA	VSS AA1	VSS AA2	VSS AA3	VSS AA4	MC1_DQ08 AA5
AB	MC0_DQ00 AB1	MC0_DQ05 AB2	MC0_DQ04 AB3	VSS AB4	MC1_DM1N AB5
AC	MC0_DM0N AC1	VSS AC2	MC0_DQ01 AC3	VSS AC4	MC1_DQ14 AC5
AD	MC0_DQ06 AD1	MC0_DQS00P AD2	MC0_DQS00N AD3	VSS AD4	MC1_DQ10 AD5
AE	MC0_DQ03 AE1	MC0_DQ02 AE2	MC0_DQ07 AE3	VSS AE4	VSS AE5
AF	VSS AF1	VSS AF2	VSS AF3	VSS AF4	MC1_DQ16 AF5
AG	MC0_DQ08 AG1	MC0_DQ13 AG2	MC0_DQ12 AG3	VSS AG4	MC1_DM2N AG5
AH	MC0_DM1N AH1	VSS AH2	MC0_DQ09 AH3	VSS AH4	MC1_DQ22 AH5
AJ	MC0_DQ14 AJ1	MC0_DQS01P AJ2	MC0_DQS01N AJ3	VSS AJ4	MC1_DQ18 AJ5
AK	MC0_DQ11 AK1	MC0_DQ10 AK2	MC0_DQ15 AK3	VSS AK4	VSS AK5
AL	VSS AL1	VSS AL2	VSS AL3	VSS AL4	MC1_DQ24 AL5
AM	MC0_DQ16 AM1	MC0_DQ21 AM2	MC0_DQ20 AM3	VSS AM4	MC1_DM3N AM5
AN	MC0_DM2N AN1	VSS AN2	MC0_DQ17 AN3	VSS AN4	MC1_DQS03N AN5
AP	MC0_DQ22 AP1	MC0_DQS02P AP2	MC0_DQS02N AP3	VSS AP4	VSS AP5
AR	MC0_DQ18 AR1	MC0_DQ23 AR2	VSS AR3	MC0_DQ28 AR4	MC0_DQ25 AR5
AT	VSS AT1	MC0_DQ19 AT2	VSS AT3	MC0_DQ29 AT4	VSS AT5
AU		VSS AU2	VSS AU3	MC0_DQ24 AU4	MC0_DM3N AU5

	6	7	8	9	10
A	HT_LDT_REQN A6	HT_RSTN A7	VSS A8	HT_TX_CLK0P A9	VSS A10
B	SE_UART0_RX B6	HT_LDT_STOPN B7	VSS B8	HT_TX_CLK0N B9	VSS B10
C	SE_QSPI_CSN C6	VSS C7	HT_TX_CTL0P C8	VSS C9	HT_TX_CAD00P C10
D	SE_QSPI_IO1 D6	VSS D7	HT_TX_CTL0N D8	VSS D9	HT_TX_CAD00N D10
E	SE_RNG0_PE E6	SE_QSPI_IO2 E7	VSS E8	HT_TX_CLK1P E9	VSS E10
F	SE_RNG1_DATA F6	HT_REXT F7	VSS F8	HT_TX_CLK1N F9	VSS F10
G	SE_GPIO03 G6	VSS G7	HT_TX_CTL1P G8	VSS G9	HT_TX_CAD08P G10
H	SPI_SCK H6	VSS H7	HT_TX_CTL1N H8	VSS H9	HT_TX_CAD08N H10
J	SPI_CSN J6	SPI_HOLDN J7	VSS J8	VDD_HT J9	VSS J10
K	UART_RXD K6	SPI_SDO K7	VSS K8	VSS K9	VDD_HT K10
L	VDD_PLL_HT L6	VSS L7	SPI_SDI L8	VSS L9	VDDP L10
M	VDD_PLL_SE M6	VDDE_IO M7	NMIN M8	VSS M9	VDDP M10
N	VSS_PLL_1V8BU N6	VDD_PLL_1V8BU N7	VSS N8	VSS N9	VDDP N10
P	VSS_PLL_1V0BU P6	VDD_PLL_1V0BU P7	VSS P8	VSS P9	VDDP P10
R	VSS R6	VSS R7	VSS R8	VSS R9	VDDP R10
T	MC1_DQ05 T6	MC1_DQ04 T7	VSS T8	VSS T9	VSS T10
U	VSS U6	MC1_DQ01 U7	VSS U8	VSS U9	VDDN U10
V	MC1_DQS0ON V6	MC1_DQ06 V7	VSS V8	VSS V9	VDDN V10
W	MC1_DQ02 W6	MC1_DQ03 W7	VSS W8	VSS W9	VSS W10
Y	VSS Y6	VSS Y7	VSS Y8	VSS Y9	VDDN Y10
AA	MC1_DQ13 AA6	MC1_DQ12 AA7	VSS AA8	VSS AA9	VDDN AA10
AB	VSS	MC1_DQ09	VSS	VSS	VDDN_SENSE-

	AB6	AB7	AB8	AB9	AB10
AC	MC1_DQS01P AC6	MC1_DQS01N AC7	VSS AC8	VSS AC9	VSS AC10
AD	MC1_DQ11 AD6	MC1_DQ15 AD7	VSS AD8	MC1_CB5 AD9	MC1_CB4 AD10
AE	VSS AE6	VSS AE7	VSS AE8	MC1_CB1 AE9	MC1_CB0 AE10
AF	MC1_DQ21 AF6	MC1_DQ20 AF7	VSS AF8	MC1_DM8N AF9	VSS AF10
AG	VSS AG6	MC1_DQ17 AG7	VSS AG8	MC1_DQS08P AG9	MC1_DQS08N AG10
AH	MC1_DQS02P AH6	MC1_DQS02N AH7	VSS AH8	MC1_CB7 AH9	MC1_CB2 AH10
AJ	MC1_DQ19 AJ6	MC1_DQ23 AJ7	VSS AJ8	VSS AJ9	VSS AJ10
AK	VSS AK6	VSS AK7	VSS AK8	VSS AK9	MC1_REXT AK10
AL	MC1_DQ25 AL6	MC1_DQ29 AL7	MC1_DQ28 AL8	VSS AL9	MC1_RESETN AL10
AM	VSS AM6	MC1_DQ30 AM7	MC1_DQ26 AM8	VSS AM9	MC1_CKE3 AM10
AN	MC1_DQS03P AN6	MC1_DQ31 AN7	MC1_DQ27 AN8	VSS AN9	VSS AN10
AP	VSS AP6	VSS AP7	VSS AP8	MC0_CB1 AP9	MC0_DQS08P AP10
AR	MC0_DQS03N AR6	MC0_DQ31 AR7	VSS AR8	MC0_CB0 AR9	MC0_DQS08N AR10
AT	MC0_DQS03P AT6	MC0_DQ26 AT7	VSS AT8	MC0_CB4 AT9	VSS AT10
AU	MC0_DQ30 AU6	MC0_DQ27 AU7	VSS AU8	MC0_CB5 AU9	MC0_DM8N AU10

	AB11	AB12	AB13		
AC	VSS AC11	VDDN AC12	VDDN AC13		
AD	VSS AD11	VDDN AD12	VDDN AD13		
AE	VSS AE11	VSS AE12	VSS AE13		
AF	VSS AF11	VSS AF12	VSS AF13		
AG	MC1_CB6 AG11	VSS AG12	VDDIO_DDR AG13	VSS AG14	VDDIO_DDR AG15
AH	MC1_CB3 AH11	VSS AH12	VSS AH13	VDDIO_DDR AH14	VSS AH15
AJ	VSS AJ11	VSS AJ12	MC1_BG1 AJ13	MC1_A08 AJ14	MC1_A04 AJ15
AK	MC1_CKE1 AK11	MC1_CKE0 AK12	MC1_ALERTN AK13	MC1_A07 AK14	VDDIO_DDR AK15
AL	VDDIO_DDR AL11	MC1_ACTN AL12	VDDIO_DDR AL13	MC1_A11 AL14	MC1_A05 AL15
AM	MC1_CKE2 AM11	MC1_BG0 AM12	MC1_A09 AM13	VDDIO_DDR AM14	MC1_A06 AM15
AN	VSS AN11	VSS AN12	MC1_A12 AN13	VDDIO_DDR AN14	VDDIO_DDR AN15
AP	MC0_CB3 AP11	VSS AP12	MC0_RESETN AP13	MC0_CKE2 AP14	MC0_BG1 AP15
AR	MC0_CB2 AR11	VSS AR12	MC0_CKE3 AR13	MC0_CKE0 AR14	MC0_A12 AR15
AT	MC0_CB7 AT11	VSS AT12	VDDIO_DDR AT13	MC0_BG0 AT14	VDDIO_DDR AT15
AU	MC0_CB6 AU11	VSS AU12	MC0_CKE1 AU13	MC0_ACTN AU14	MC0_ALERTN AU15

	16	17	18	19	20
A		HT_TX_CAD07P A17		HT_RX_CLK0N A19	
B	VSS B16	HT_TX_CAD07N B17	VSS B18	HT_RX_CLK0P B19	VSS B20
C	HT_TX_CAD06P C16	VSS C17	HT_RX_CTL0N C18	VSS C19	HT_RX_CAD00N C20
D	HT_TX_CAD06N D16	VSS D17	HT_RX_CTL0P D18	VSS D19	HT_RX_CAD00P D20
E	VSS E16	HT_TX_CAD15P E17	VSS E18	HT_RX_CLK1P E19	VSS E20
F	VSS F16	HT_TX_CAD15N F17	VSS F18	HT_RX_CLK1N F19	VSS F20
G	HT_TX_CAD14P G16	VSS G17	HT_RX_CTL1P G18	VSS G19	HT_RX_CAD08P G20
H	HT_TX_CAD14N H16	VSS H17	HT_RX_CTL1N H18	VSS H19	HT_RX_CAD08N H20
J	VSS J16	VDD_HT J17	VSS J18	VDD_HT J19	VSS J20
K	VDD_HT K16	VSS K17	VDD_HT K18	VSS K19	VDD_HT K20
L	VDDP L16	VDDP L17	VDDP L18	VDDP L19	VDDP L20
M					
N					
P					
R					
T					
U					
V					
W					
Y					
AA					
AB					
AC					
AD					
AE					
AF					
AG	VSS AG16	VDD_PHY_DDR AG17	VDD_PHY_DDR AG18	VDD_PHY_DDR AG19	VDD_PHY_DDR AG20
AH	VDDIO_DDR AH16	VSS AH17	VSS AH18	VSS AH19	VSS AH20
AJ	VDDIO_DDR	MC1_CK1N	VDDIO_DDR	MC1_CK2N	VDDIO_DDR

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AB				AA25 VDDN AB25
AC				VDDN AC25 VDDN AD25
AD				
AE				VSS AE25 VSS AF25
AF				
AG	VDD_PHY_DDR AG21	VSS AG22	VSS AG24	VDD_PHY_DDR AG25
AH	VSS AH21	VDDIO_DDR AH22	VDDIO_DDR AH24	VSS AH25
AJ	VDDIO_DDR AJ21	MC1_SCSN2 AJ22	MC1_A17 AJ24	VDDIO_DDR AJ25
AK	MC1_RASN AK21	VDDIO_DDR AK22	VDDIO_DDR AK24	MC1_ODT3 AK25
AL	MC1_BA0 AL21	MC1_WEN AL22		

	26	27	28	29	30
A	VSS A26	HT_RX_CAD07N A27	VSS A28	VDDP A29	VDDP A30
B	VSS B26	HT_RX_CAD07P B27	VSS B28	VDDP B29	VDDP B30
C	HT_RX_CAD06N C26	VSS C27	HT_CLKN C28	VSS C29	VDDP C30
D	HT_RX_CAD06P D26	VSS D27	HT_CLKP D28	VSS D29	VDDP D30
E	VSS E26	HT_RX_CAD15P E27	VSS E28	VDDP E29	VDDP E30
F	VSS F26	HT_RX_CAD15N F27	VSS F28	VDDP F29	VDDP F30
G	HT_RX_CAD14P G26	VSS G27	VSS G28	VDDP G29	VDDP G30
H	HT_RX_CAD14N H26	VSS H27	VSS H28	VDDP H29	VDDP H30
J	VSS J26	VDDP J27	VDDP J28	VDDP J29	VDDP J30
K	VDDP K26	VDDP K27	VSS K28	VDDP K29	VSS K30
L	VDDP L26	VDDP L27	VDDP L28	VSS L29	VDDN L30
M	VSS M26	VDDP M27	VSS M28	VDDN M29	VDDN M30
N	VSS N26	VSS N27	VDDN N28	VDDN N29	VDDN N30
P	VDDN P26	VDDN P27	VDDN P28	VDDN P29	VSS P30
R	VDDN R26	VDDN R27	VDDN R28	VDDN R29	VDDN R30
T	VDDN T26	VDDN T27	VDDN T28	VDDN T29	VDDN T30
U	VDDN U26	VSS U27	VSS U28	VSS U29	VSS U30
V	VDDN V26	VDDN V27	VDDN V28	VDDN V29	VDDN V30
W	VDDN W26	VDDN W27	VDDN W28	VDDN W29	VDDN W30
Y	VDDN Y26	VDDN Y27	VDDN Y28	VSS Y29	VSS Y30
AA	VDDN AA26	VDDN AA27	VSS AA28	VSS AA29	MC1_DQ59 AA30
AB	VDDN	VSS	VSS	VSS	MC1_DQS07P

Net Name	Conductor Length (um)
HT_RX_CAD00N	19725.756
HT_RX_CAD00P	19768.68
HT_RX_CAD01N	19691.224
HT_RX_CAD01P	19734.148
HT_RX_CAD02N	19646.261
HT_RX_CAD02P	19689.185
HT_RX_CAD03N	19724.373
HT_RX_CAD03P	19767.297
HT_RX_CAD04N	19605.848
HT_RX_CAD04P	19648.772
HT_RX_CAD05N	19728.393
HT_RX_CAD05P	19771.317
HT_RX_CAD06N	19656.961
HT_RX_CAD06P	19697.207

HT_RX_CTL0P	19693.683
HT_RX_CTL1N	19609.49
HT_RX_CTL1P	19636.557
HT_TX_CAD00N	24841.845
HT_TX_CAD00P	24881.728
HT_TX_CAD01N	24885.068
HT_TX_CAD01P	24930.916
HT_TX_CAD02N	24821.225
HT_TX_CAD02P	24861.108
HT_TX_CAD03N	24807.051
HT_TX_CAD03P	24855.162
HT_TX_CAD04N	24790.656
HT_TX_CAD04P	24830.539
HT_TX_CAD05N	24794.284
HT_TX_CAD05P	24815.279
HT_TX_CAD06N	24806.327
HT_TX_CAD06P	24843.906
HT_TX_CAD07N	24857.139
HT_TX_CAD07P	24902.986
HT_TX_CAD08N	24894.115
HT_TX_CAD08P	24932.341
HT_TX_CAD09N	24878.895
HT_TX_CAD09P	24919.109
HT_TX_CAD10N	24787.507
HT_TX_CAD10P	24819.023
HT_TX_CAD11N	24821.277
HT_TX_CAD11P	24867.166
HT_TX_CAD12N	24814.684
HT_TX_CAD12P	24849.95
HT_TX_CAD13N	24786.215
HT_TX_CAD13P	24812.429
HT_TX_CAD14N	24958.103
HT_TX_CAD14P	24917.2
HT_TX_CAD15N	24792.489
HT_TX_CAD15P	24805.095
HT_TX_CLK0N	24844.085
HT_TX_CLK0P	24871.859
HT_TX_CLK1N	24853.75
HT_TX_CLK1P	24819.405
HT_TX_CTL0N	24794.294
HT_TX_CTL0P	24834.177
HT_TX_CTL1N	24887.652

HT_TX_CTL1P	24848.169
MC0_A00	16677.264
MC0_A01	16711.907
MC0_A02	16709.824
MC0_A03	16723.271
MC0_A04	16714.412
MC0_A05	16701.275
MC0_A06	16739.256
MC0_A07	16751.871
MC0_A08	16749.37
MC0_A09	16735.709
MC0_A10	16709.377
MC0_A11	16732.479
MC0_A12	16728.901
MC0_A13	16735.503
MC0_A17	16735.523
MC0_ACTN	16754.93
MC0_ALERTN	16724.656
MC0_BA0	16755.549
MC0_BA1	16739.634
MC0_BG0	16704.839
MC0_BG1	16736.822
MC0_CASN	16751.741
MC0_CB0	17628.548
MC0_CB1	17661.191
MC0_CB2	17633.791
MC0_CB3	17597.016
MC0_CB4	17597.199
MC0_CB5	17622.1
MC0_CB6	17626.458
MC0_CB7	17580.124
MC0_CK0N	16822.905
MC0_CK0P	16823.023
MC0_CK1N	16737.138
MC0_CK1P	16729.792
MC0_CK2N	16823.476
MC0_CK2P	16818.12
MC0_CK3N	16808.18
MC0_CK3P	16805.461
MC0_CKE0	16709.536
MC0_CKE1	16725.297
MC0_CKE2	16668.417

MC0_CKE3	16729.033
MC0_DM0N	13961.953
MC0_DM1N	16950.611
MC0_DM2N	20511.914
MC0_DM3N	20276.562
MC0_DM4N	17950.779
MC0_DM5N	19607.741
MC0_DM6N	17013.839
MC0_DM7N	14286.483
MC0_DM8N	17586.295
MC0_DQ00	13970.54
MC0_DQ01	13933.533
MC0_DQ02	13960.408
MC0_DQ03	13961.392
MC0_DQ04	13973.737
MC0_DQ05	13962.222
MC0_DQ06	13960.409
MC0_DQ07	14008.071
MC0_DQ08	16981.6
MC0_DQ09	16958.885
MC0_DQ10	16988.822
MC0_DQ11	16945.336
MC0_DQ12	16941.554
MC0_DQ13	16980.148
MC0_DQ14	16952.004
MC0_DQ15	16960.234
MC0_DQ16	20502.042
MC0_DQ17	20524.667
MC0_DQ18	20512.058
MC0_DQ19	20583.795
MC0_DQ20	20518.992
MC0_DQ21	20516.791
MC0_DQ22	20546.088
MC0_DQ23	20522.411
MC0_DQ24	20283.919
MC0_DQ25	20248.695
MC0_DQ26	20230.653
MC0_DQ27	20263.584
MC0_DQ28	20293.638
MC0_DQ29	20303.87
MC0_DQ30	20285.33
MC0_DQ31	20217.949

MC0_DQ32	17848.383
MC0_DQ33	17910.261
MC0_DQ34	17884.473
MC0_DQ35	17933.651
MC0_DQ36	17897.674
MC0_DQ37	17818.992
MC0_DQ38	17897.885
MC0_DQ39	17864.32
MC0_DQ40	19656.583
MC0_DQ41	19648.457
MC0_DQ42	19647.217
MC0_DQ43	19648.733
MC0_DQ44	19626.113
MC0_DQ45	19616.819
MC0_DQ46	19618.068
MC0_DQ47	19620.287
MC0_DQ48	17062.169
MC0_DQ49	17039.177
MC0_DQ50	17005.618
MC0_DQ51	17034.421
MC0_DQ52	17052.462
MC0_DQ53	16970.908
MC0_DQ54	17051.492
MC0_DQ55	17033.951
MC0_DQ56	14241.709
MC0_DQ57	14250.735
MC0_DQ58	14285.628
MC0_DQ59	14277.354
MC0_DQ60	14223.206
MC0_DQ61	14279.796
MC0_DQ62	14244.032
MC0_DQ63	14282.275
MC0_DQS00N	14036.303
MC0_DQS00P	14027.285
MC0_DQS01N	17018.476
MC0_DQS01P	17010.269
MC0_DQS02N	20528.914
MC0_DQS02P	20533.624
MC0_DQS03N	20325.58
MC0_DQS03P	20313.318
MC0_DQS04N	17928.36
MC0_DQS04P	17916.011

MC1_CASN	13723.335
MC1_CB0	14190.922
MC1_CB1	14278.193
MC1_CB2	14240.562
MC1_CB3	14268.084
MC1_CB4	14264.42
MC1_CB5	14172.775
MC1_CB6	14311.986
MC1_CB7	14233.866
MC1_CKON	13773.623
MC1_CKOP	13770.37
MC1_CK1N	13682.334
MC1_CK1P	13693.492
MC1_CK2N	138598

MC1_DQ12	12588.178
MC1_DQ13	12609.183
MC1_DQ14	12622.902
MC1_DQ15	12578.846
MC1_DQ16	14390.617
MC1_DQ17	14347.39
MC1_DQ18	14350.483
MC1_DQ19	14366.286
MC1_DQ20	[redacted]
MC1_DQ21	14342.757
MC1_DQ22	14361.89
MC1_DQ23	14415.492
MC1_DQ24	17274.746
MC1_DQ25	17128.96
MC1_DQ26	[redacted]
MC1_DQ27	

V1.0		
V1.1	9.3	
V1.2	LL 1.15V	
	1. 2.3.4 2.3.6	
	2. 9.2 VDDP 0.95V VDDN VDDP	
V1.3	3. 10.1.2	
	4. 11.2	
	5. 11.3 M	
	1. 1.1 “ ” “ ”	
	2. 1.5 7.1 7.2 9.2 11.1 11.2 BLL	
V1.4		
	3. 9.1 VDD_PLL_1V0BU	
	4. 9.2	